# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

# HEF4520B
# MSI
# Dual binary counter

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

# DUAL BINARY COUNTER

The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input ($CP_0$) and an active LOW clock input ($\overline{CP}_1$), buffered outputs from all four bit positions ($O_0$ to $O_3$) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the $CP_0$ input if $\overline{CP}_1$ is HIGH or the HIGH to LOW transition of the $\overline{CP}_1$ input if $CP_0$ is LOW. Either $CP_0$ or $\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter ($O_0$ to $O_3$ = LOW) independent of $CP_0$, $\overline{CP}_1$.
Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

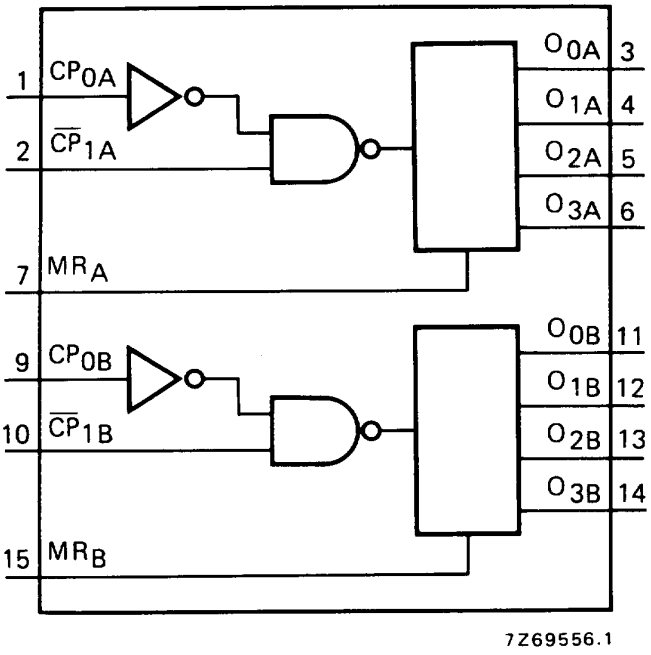


Fig. 1 Functional diagram.

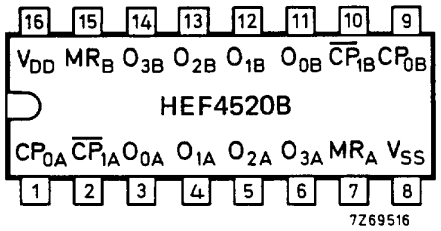


Fig. 2 Pinning diagram.

HEF4520BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4520BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4520BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

## PINNING

| | |
|---|---|
| $CP_{0A}$, $CP_{0B}$ | clock inputs (L to H triggered) |
| $\overline{CP}_{1A}$, $\overline{CP}_{1B}$ | clock inputs (H to L triggered) |
| $MR_A$, $MR_B$ | master reset inputs |
| $O_{0A}$ to $O_{3A}$ | outputs |
| $O_{0B}$ to $O_{3B}$ | outputs |

**FAMILY DATA**

**$I_{DD}$ LIMITS category MSI**

} see Family Specifications

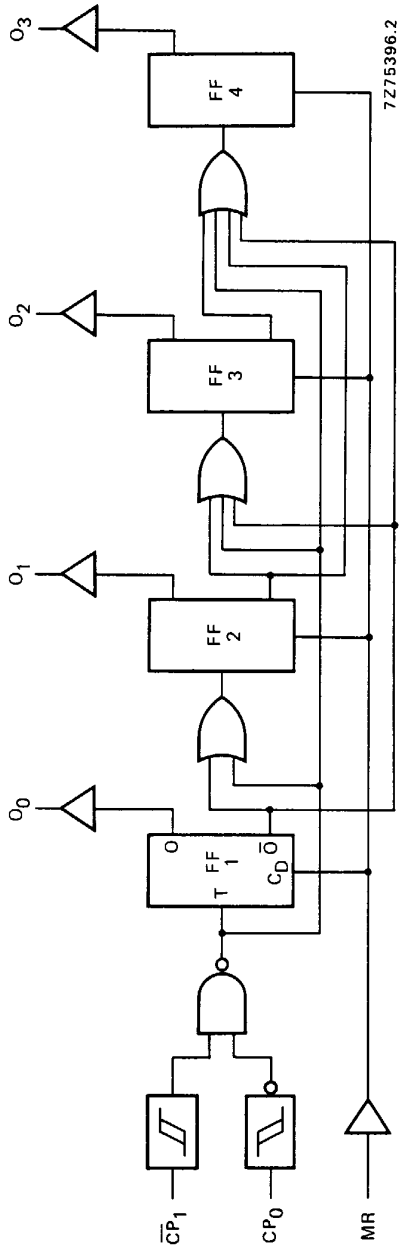


Fig. 3 Logic diagram (one counter).

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌣ = negative-going transition

**FUNCTION TABLE**

| $CP_0$ | $\overline{CP}_1$ | MR | mode |
|---|---|---|---|
| ∫ | H | L | counter advances |
| L | ⌣ | L | counter advances |
| ⌣ | X | L | no change |
| X | ∫ | L | no change |
| ∫ | L | L | no change |
| H | ⌣ | L | no change |
| X | X | H | $O_0$ to $O_3$ = LOW |

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ⩽ 20 ns

| | $V_{DD}$ V | symbol | min. | typ. | max. | | typical extrapolation formula |
|---|---|---|---|---|---|---|---|
| Propagation delays | | | | | | | |
| $CP_0$, $\overline{CP}_1$ → $O_n$ | 5 | | | 110 | 220 | ns | 83 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 110 | 220 | ns | 83 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| MR → $O_n$ | 5 | | | 75 | 150 | ns | 48 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 35 | 70 | ns | 24 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) $C_L$ |
| Output transition times | | | | | | | |
| | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{THL}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{TLH}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| Minimum $CP_0$ | 5 | | 60 | 30 | | ns | see also waveforms Figs 4 and 5 |
| pulse width; LOW | 10 | $t_{WCPL}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| Minimum $\overline{CP}_1$ | 5 | | 60 | 30 | | ns | |
| pulse width; HIGH | 10 | $t_{WCPH}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| Minimum MR | 5 | | 30 | 15 | | ns | |
| pulse width; HIGH | 10 | $t_{WMRH}$ | 20 | 10 | | ns | |
| | 15 | | 16 | 8 | | ns | |
| Recovery time | 5 | | 50 | 25 | | ns | |
| for MR | 10 | $t_{RMR}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| Set-up times | 5 | | 50 | 25 | | ns | |
| $CP_0$ → $\overline{CP}_1$ | 10 | $t_{su}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| | 5 | | 50 | 25 | | ns | |
| $\overline{CP}_1$ → $CP_0$ | 10 | $t_{su}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| Maximum clock | 5 | | 8 | 16 | | MHz | |
| pulse frequency | 10 | $f_{max}$ | 15 | 30 | | MHz | |
| | 15 | | 20 | 40 | | MHz | |

## A.C. CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; input transition times ⩽ 20 ns

| | $V_{DD}$ V | typical formula for P (μW) | where |
|---|---|---|---|
| Dynamic power dissipation per package (P) | 5 | $850f_i + \Sigma(f_oC_L) \times V_{DD}^2$ | $f_i$ = input freq. (MHz)<br>$f_o$ = output freq. (MHz)<br>$C_L$ = load capacitance (pF)<br>$\Sigma(f_oC_L)$ = sum of outputs<br>$V_{DD}$ = supply voltage (V) |
| | 10 | $3\,800f_i + \Sigma(f_oC_L) \times V_{DD}^2$ | |
| | 15 | $10\,200f_i + \Sigma(f_oC_L) \times V_{DD}^2$ | |

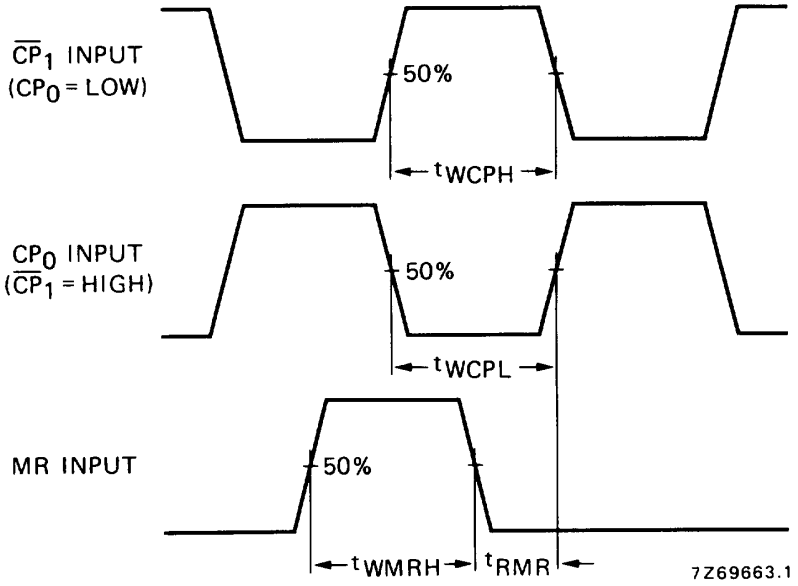


Fig. 4 Waveforms showing recovery time for MR; minimum $CP_0$, $\overline{CP}_1$ and MR pulse widths.

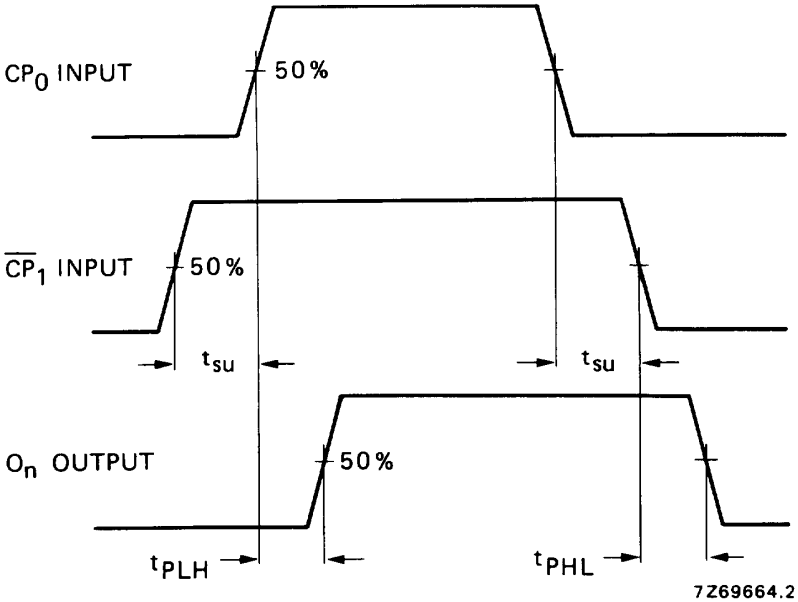


Fig. 5 Waveforms showing set-up times for $CP_0$ to $\overline{CP}_1$ and $\overline{CP}_1$ to $CP_0$, and propagation delays.

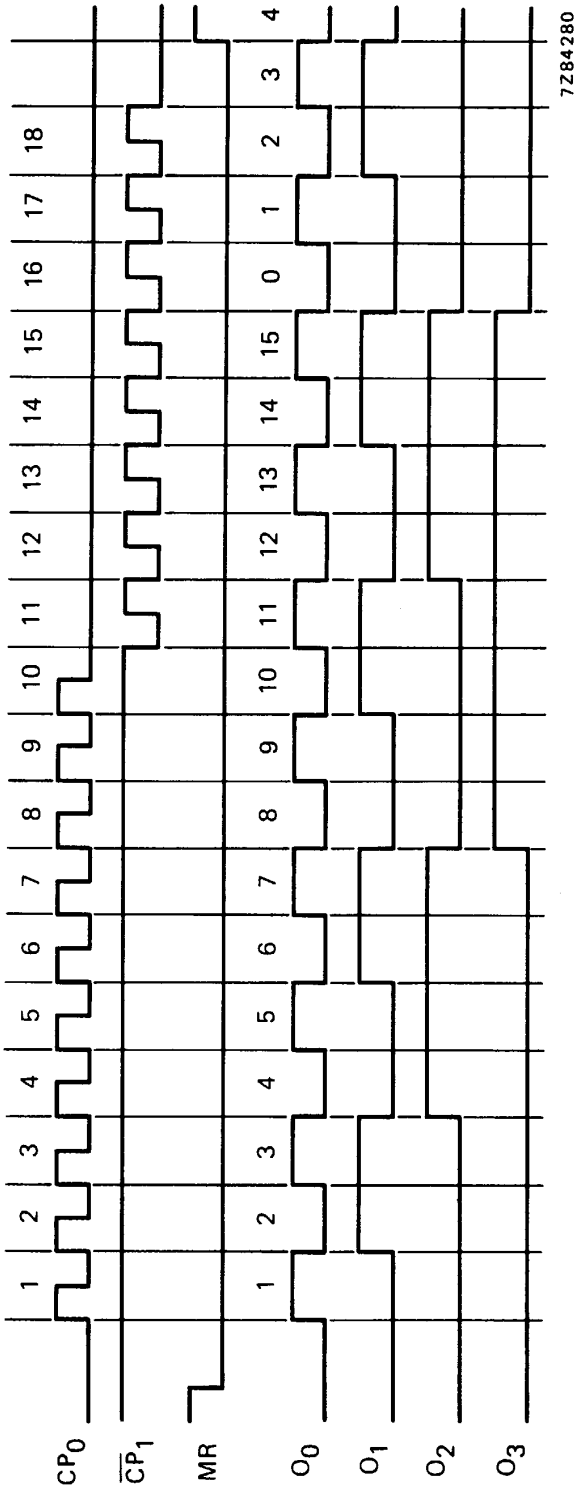


Fig. 6 Timing diagram.