

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4093B

gates

Quadruple 2-input NAND Schmitt trigger

Product specification
File under Integrated Circuits, IC04

January 1995

Quadruple 2-input NAND Schmitt trigger

HEF4093B gates

DESCRIPTION

The HEF4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H).

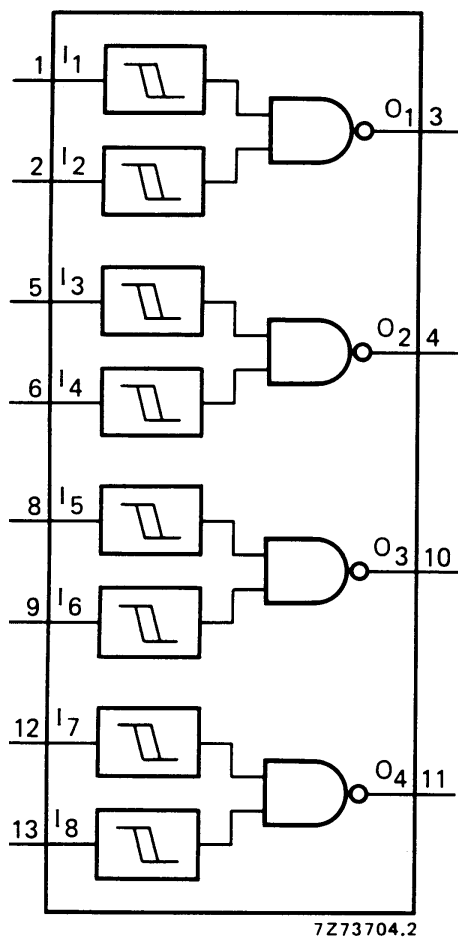


Fig.1 Functional diagram.

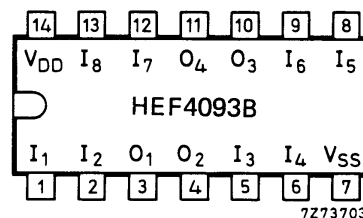


Fig.2 Pinning diagram.

HEF4093BP(N): 14-lead DIL; plastic
(SOT27-1)

HEF4093BD(F): 14-lead DIL; ceramic (cerdip)
(SOT73)

HEF4093BT(D): 14-lead SO; plastic
(SOT108-1)

(): Package Designator North America

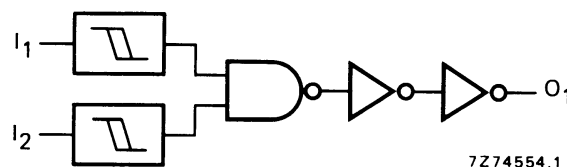


Fig.3 Logic diagram (one gate).

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

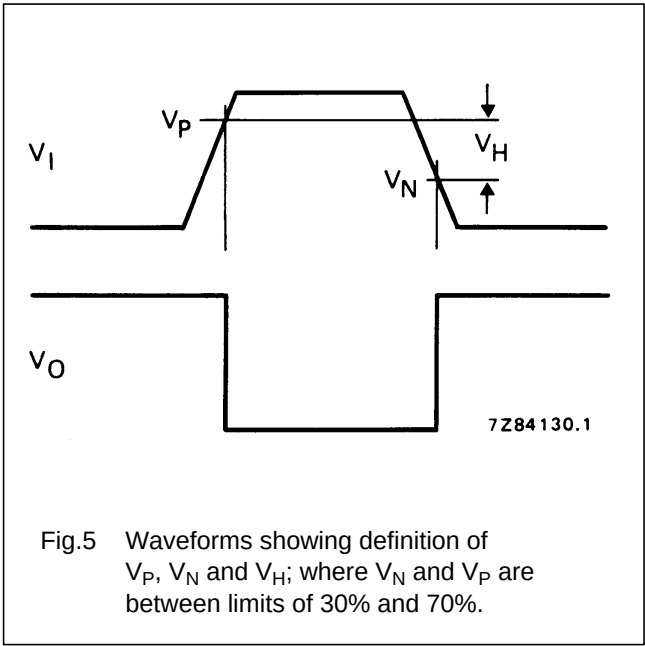
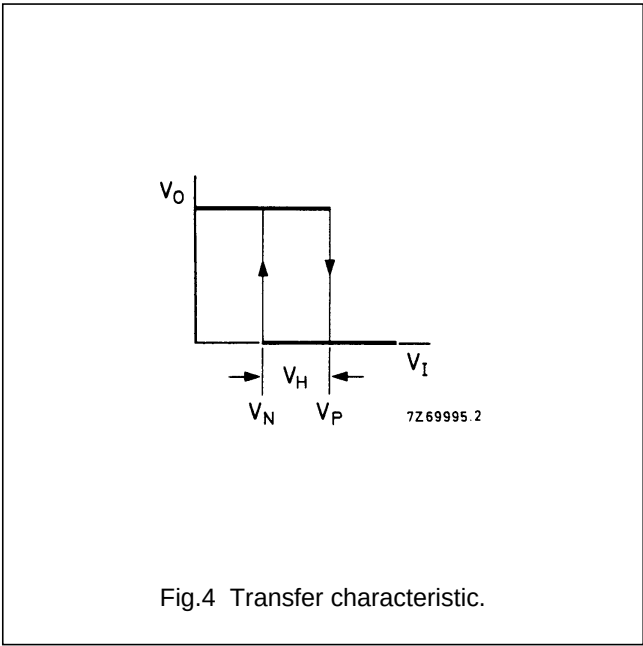
Quadruple 2-input NAND Schmitt trigger

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DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.
Hysteresis voltage	5	V_H	0,4	0,7	–
	10		0,6	1,0	–
	15		0,7	1,3	–
Switching levels positive-going input voltage	5	V_P	1,9	2,9	3,5
	10		3,6	5,2	7
	15		4,7	7,3	11
negative-going input voltage	5	V_N	1,5	2,2	3,1
	10		3	4,2	6,4
	15		4	6,0	10,3



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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	90	185 ns	63 ns + (0,55 ns/pF) C_L
	10		40	80 ns	29 ns + (0,23 ns/pF) C_L
	15		30	60 ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PLH}	85	170 ns	58 ns + (0,55 ns/pF) C_L
	10		40	80 ns	29 ns + (0,23 ns/pF) C_L
	15		30	60 ns	22 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5	t_{THL}	60	120 ns	10 ns + (1,0 ns/pF) C_L
	10		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15		20	40 ns	6 ns + (0,28 ns/pF) C_L
	5	t_{TLH}	60	120 ns	10 ns + (1,0 ns/pF) C_L
	10		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15		20	40 ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5	$1300 f_i + \sum(f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6400 f_i + \sum(f_o C_L) \times V_{DD}^2$	
	15	$18\,700 f_i + \sum(f_o C_L) \times V_{DD}^2$	

Quadruple 2-input NAND Schmitt trigger

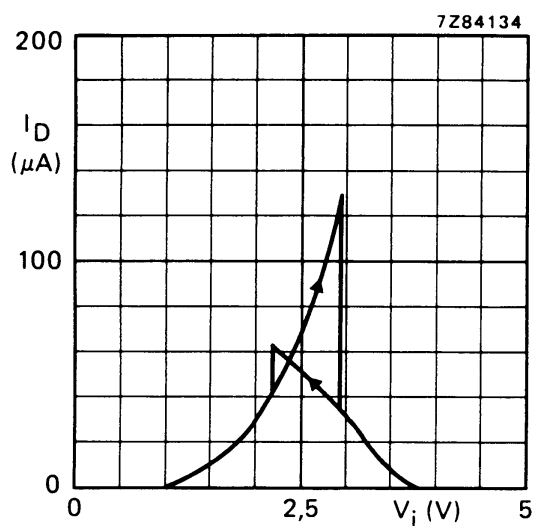
HEF4093B
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Fig.6 Typical drain current as a function of input voltage; $V_{DD} = 5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

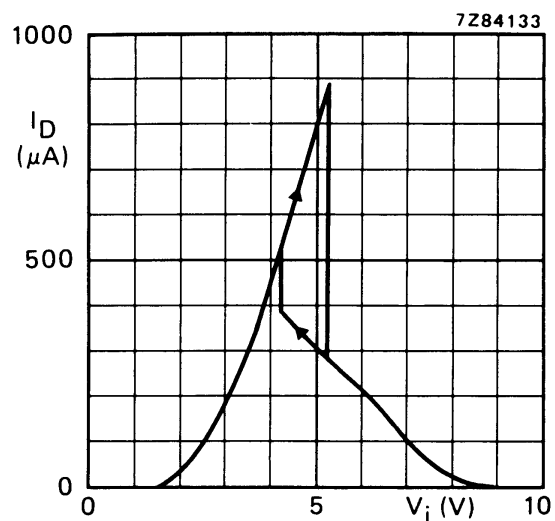


Fig.7 Typical drain current as a function of input voltage; $V_{DD} = 10\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

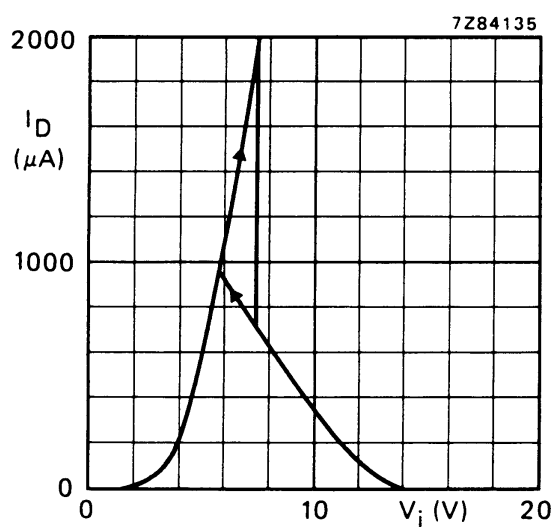


Fig.8 Typical drain current as a function of input voltage; $V_{DD} = 15\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

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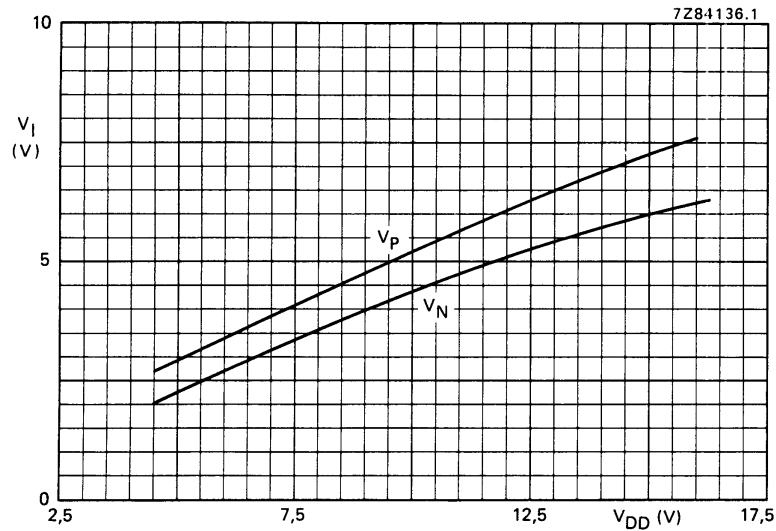


Fig.9 Typical switching levels as a function of supply voltage V_{DD} ; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

APPLICATION INFORMATION

Some examples of applications for the HEF4093B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

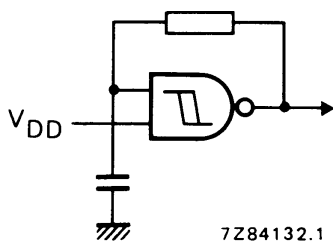


Fig.10 The HEF4093B used as a astable multivibrator.

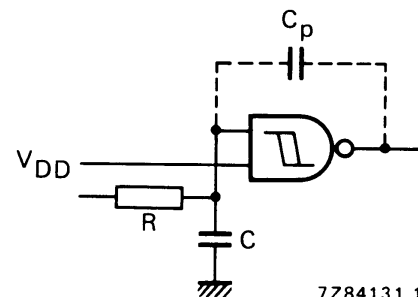


Fig.11 Schmitt trigger driven via a high impedance ($R > 1\text{ k}\Omega$).

If a Schmitt trigger is driven via a high impedance ($R > 1\text{ k}\Omega$) then it is necessary to incorporate a capacitor C of such value that:

$$\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}, \text{ otherwise oscillation can occur on the edges of a pulse.}$$

C_p is the external parasitic capacitance between inputs and output; the value depends on the circuit board layout.

Note

The two inputs may be connected together, but this will result in a larger through-current at the moment of switching.

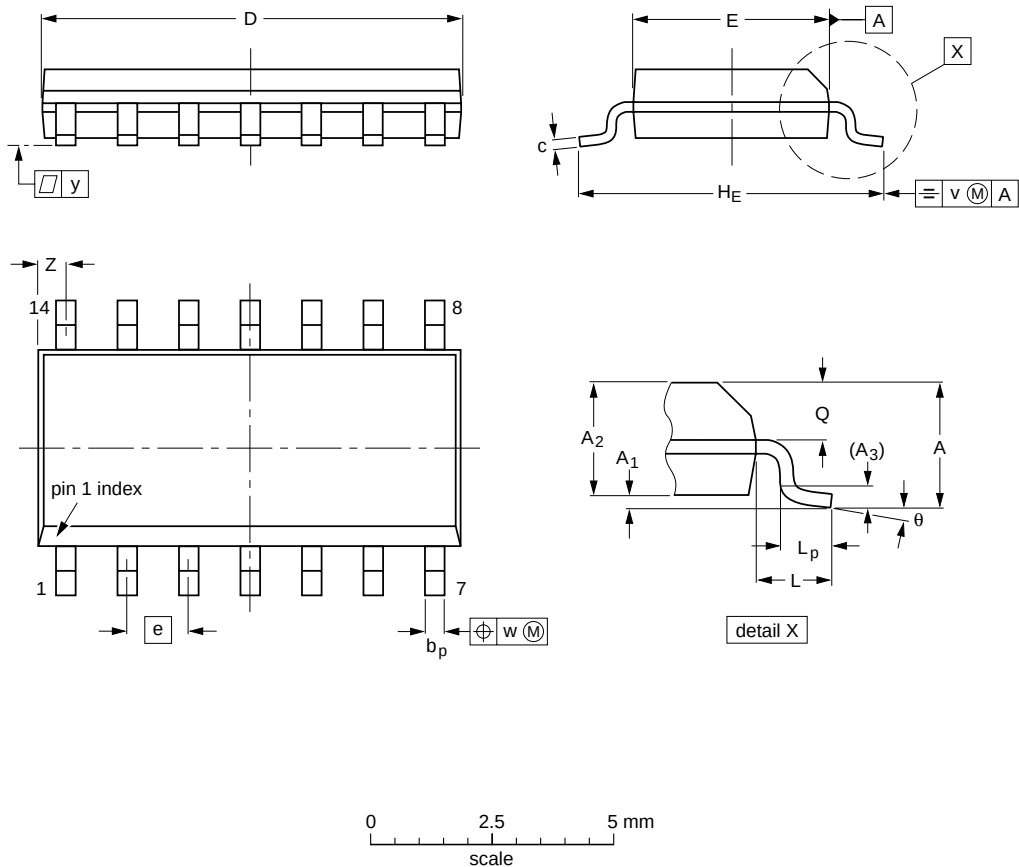
Package information

Package outlines

SO

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22

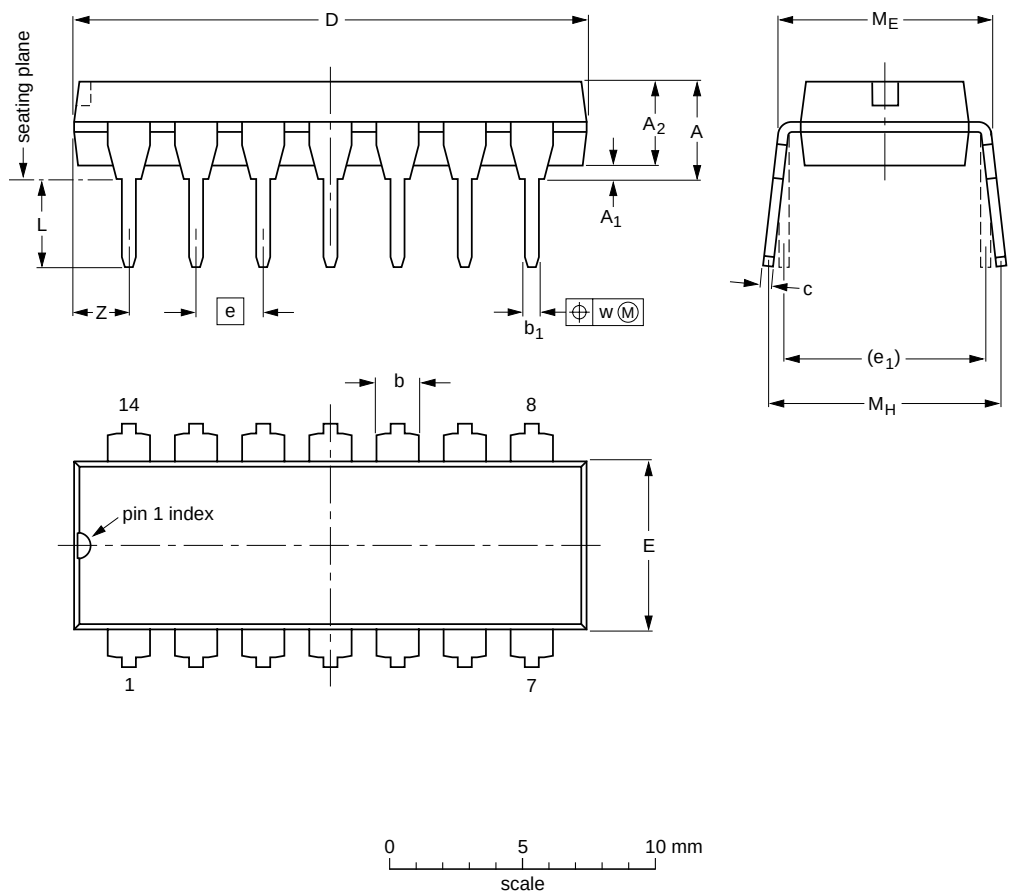
Package information

Package outlines

DIP

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11