

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4069UB **gates** **Hex inverter**

Product specification
File under Integrated Circuits, IC04

January 1995

Hex inverter

HEF4069UB
gates

DESCRIPTION

The HEF4069UB is a general purpose hex inverter. Each of the six inverters is a single stage.

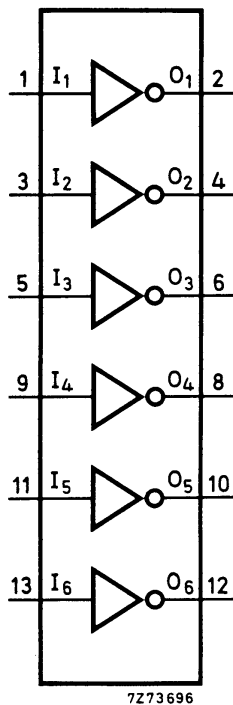


Fig.1 Functional diagram.

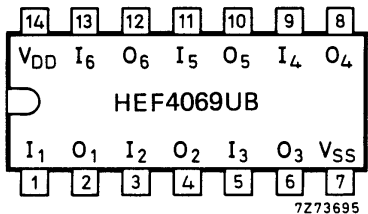


Fig.2 Pinning diagram.

- HEF4069UBP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4069UBD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4069UBT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America

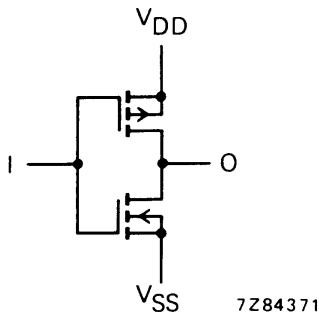


Fig.3 Schematic diagram (one inverter).

FAMILY DATA, I_{DD} LIMITS category GATES
See Family Specifications for V_{IH}/V_{IL} unbuffered stages

Hex inverter

HEF4069UB
gates

AC CHARACTERISTICS

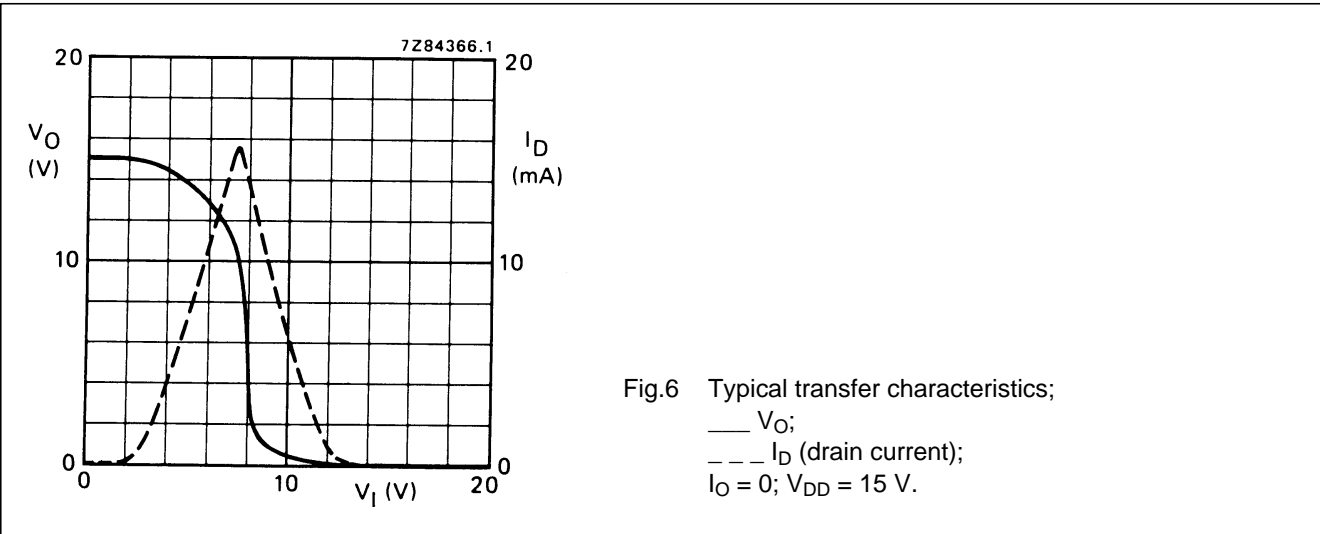
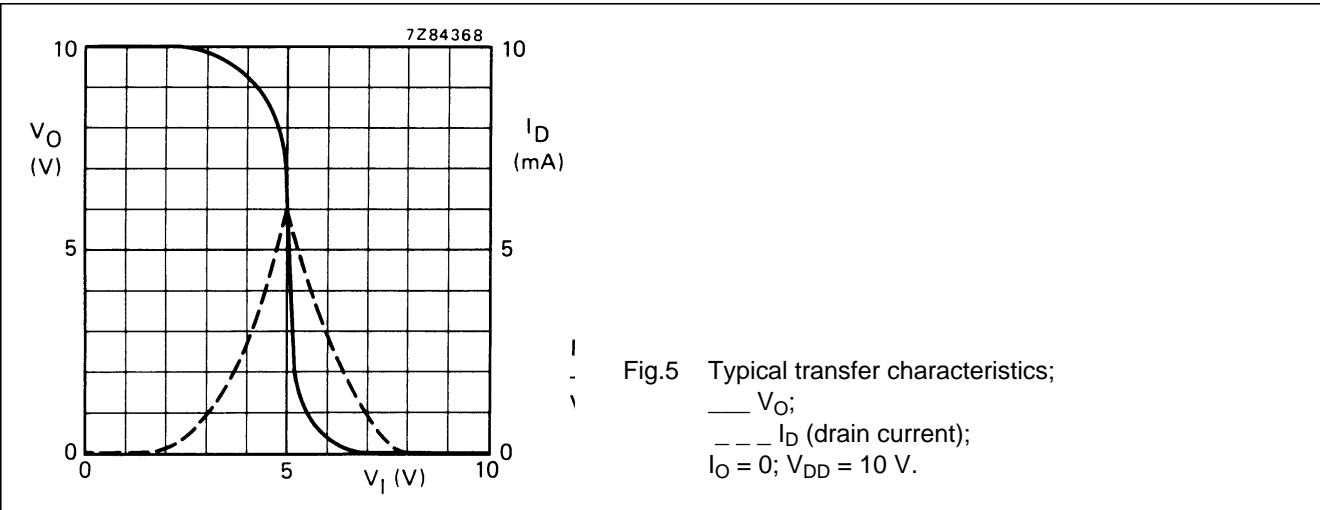
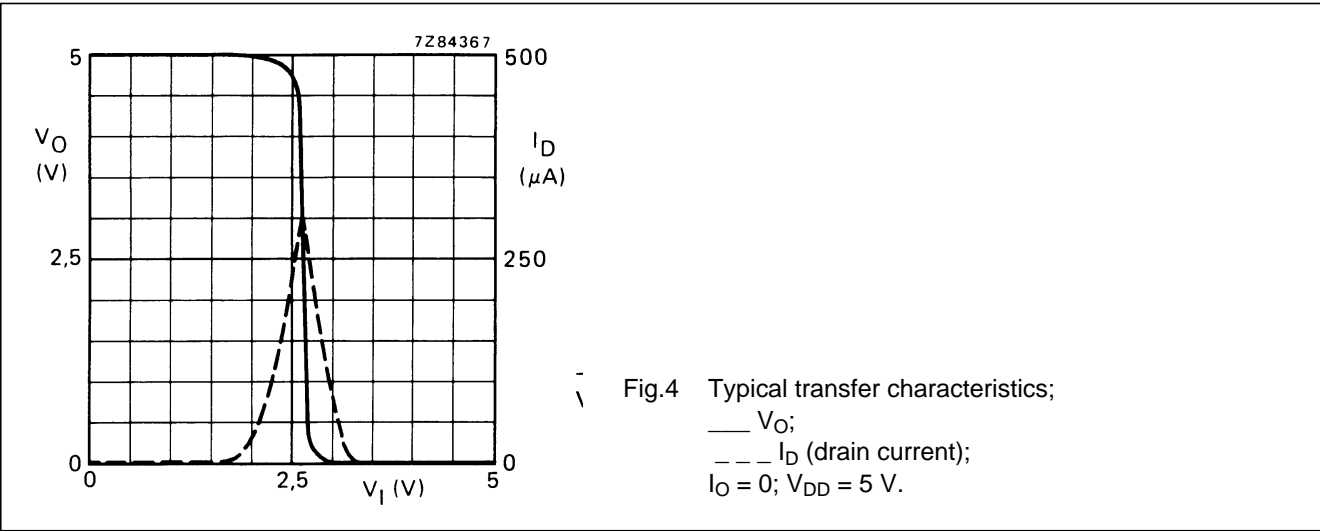
$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW LOW to HIGH	5	t_{PHL}	45	90 ns	18 ns + (0,55 ns/pF) C_L
	10		20	40 ns	9 ns + (0,23 ns/pF) C_L
	15		15	25 ns	7 ns + (0,16 ns/pF) C_L
	5	t_{PLH}	40	80 ns	13 ns + (0,55 ns/pF) C_L
	10		20	40 ns	9 ns + (0,23 ns/pF) C_L
	15		15	30 ns	7 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW LOW to HIGH	5	t_{THL}	60	120 ns	10 ns + (1,0 ns/pF) C_L
	10		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15		20	40 ns	6 ns + (0,28 ns/pF) C_L
	5	t_{TLH}	60	120 ns	10 ns + (1,0 ns/pF) C_L
	10		30	60 ns	9 ns + (0,42 ns/pF) C_L
	15		20	40 ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5	$600 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$22\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

Hex inverter

HEF4069UB
gates



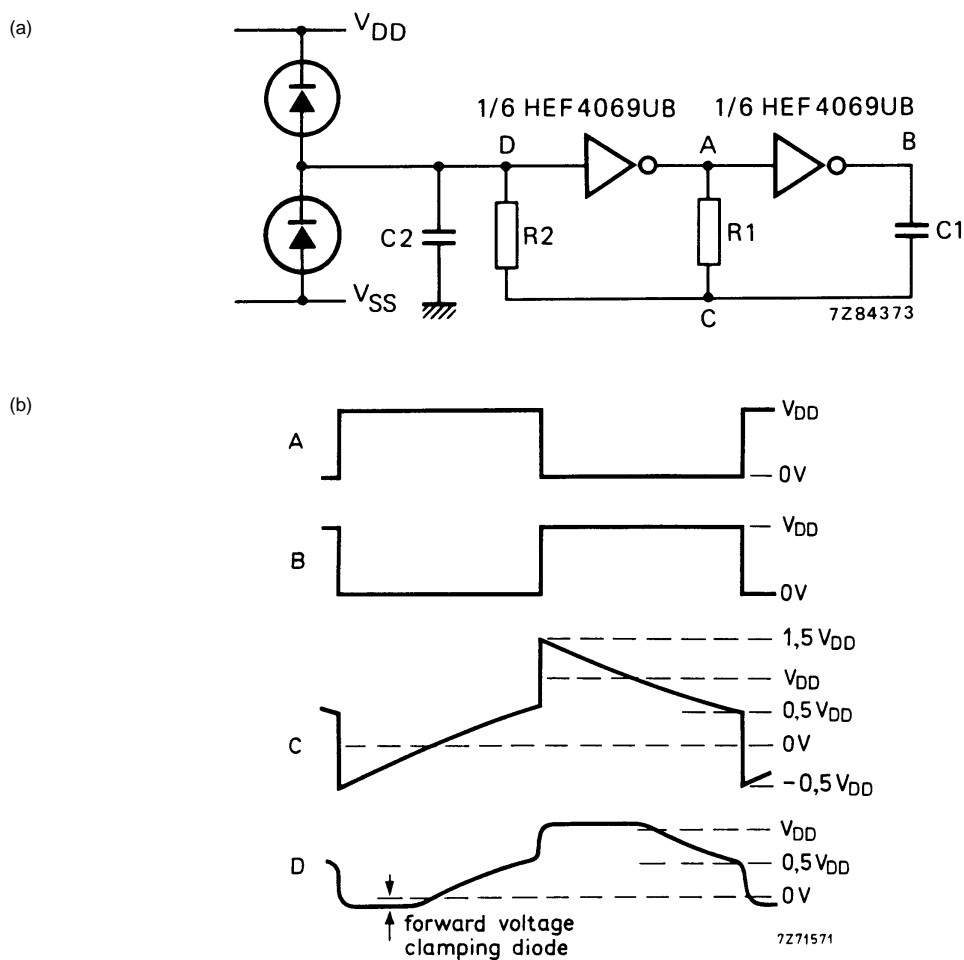
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HEF4069UB
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APPLICATION INFORMATION

Some examples of applications for the HEF4069UB are shown below.

In Fig.7 an astable relaxation oscillator is given. The oscillation frequency is mainly determined by $R1C1$, provided $R1 \ll R2$ and $R2C2 \ll R1C1$.



The function of $R2$ is to minimize the influence of the forward voltage across the protection diodes on the frequency; $C2$ is a stray (parasitic) capacitance. The period T_p is given by $T_p = T_1 + T_2$, in which

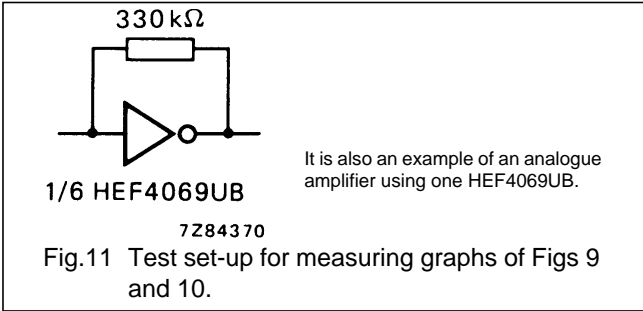
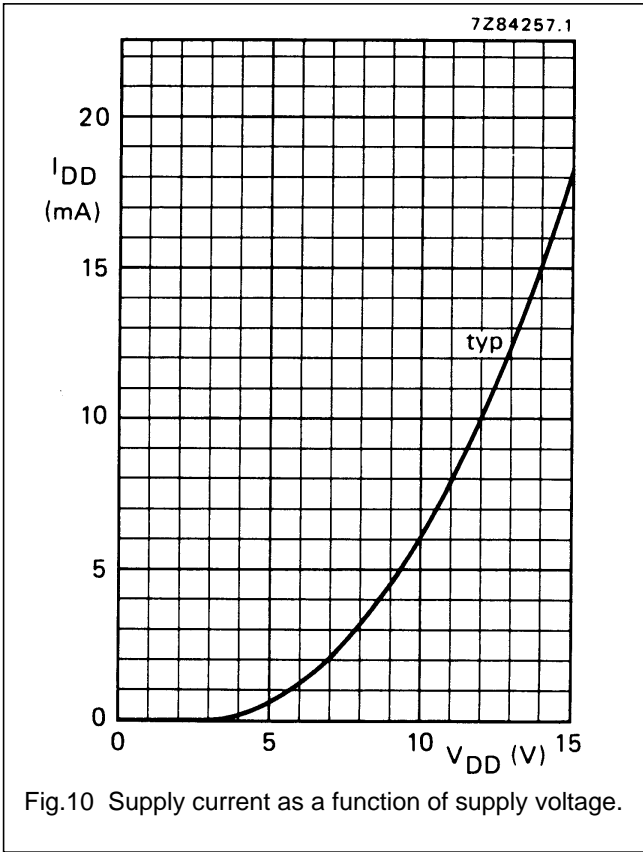
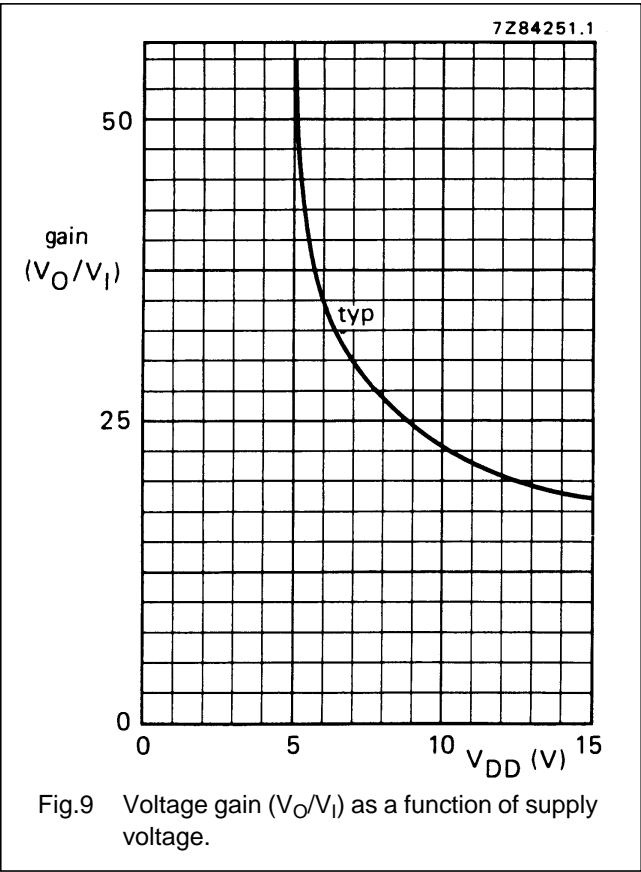
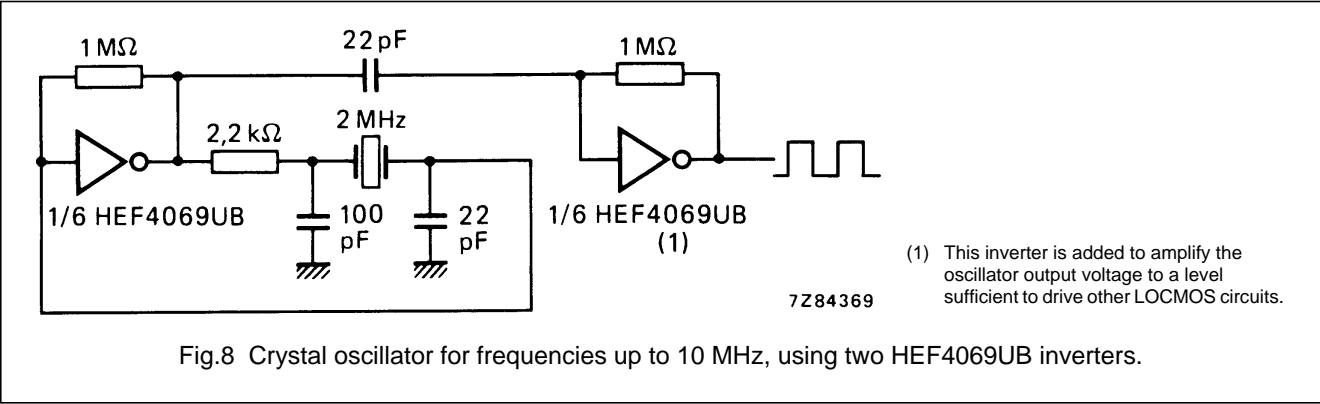
$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

V_{ST} is the signal threshold level of the inverter. The period is fairly independent of V_{DD} , V_{ST} and temperature. The duty factor, however, is influenced by V_{ST} .

Fig.7 (a) Astable relaxation oscillator using two HEF4069UB inverters; the diodes may be BAW62; $C2$ is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

Hex inverter

HEF4069UB
gates



Hex inverter

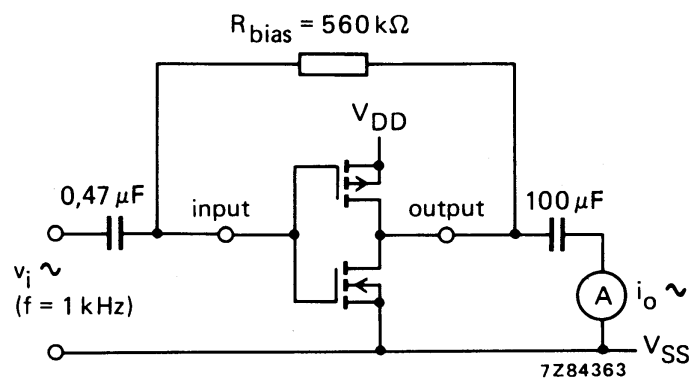
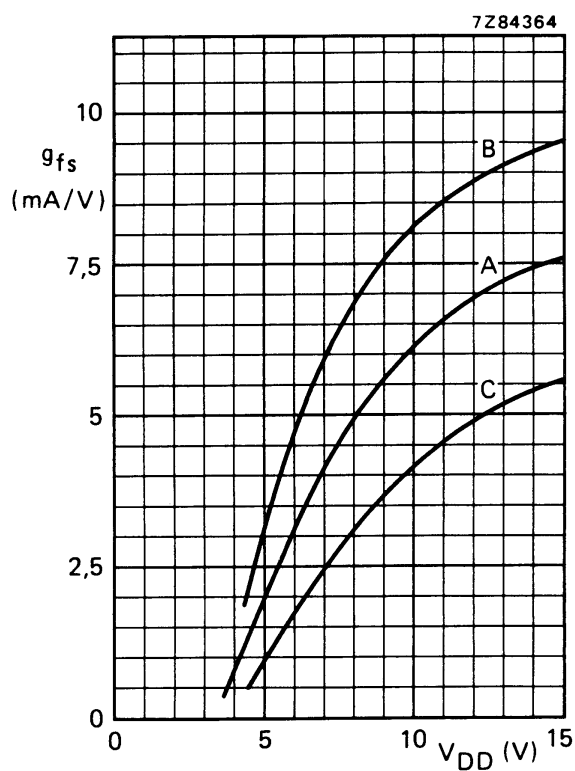
HEF4069UB
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Fig.12 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.13).



A : average,
B : average + 2 s,
C : average - 2 s, where:
's' is the observed standard
deviation.

Fig.13 Typical forward transconductance g_{fs} as a function of the supply voltage at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

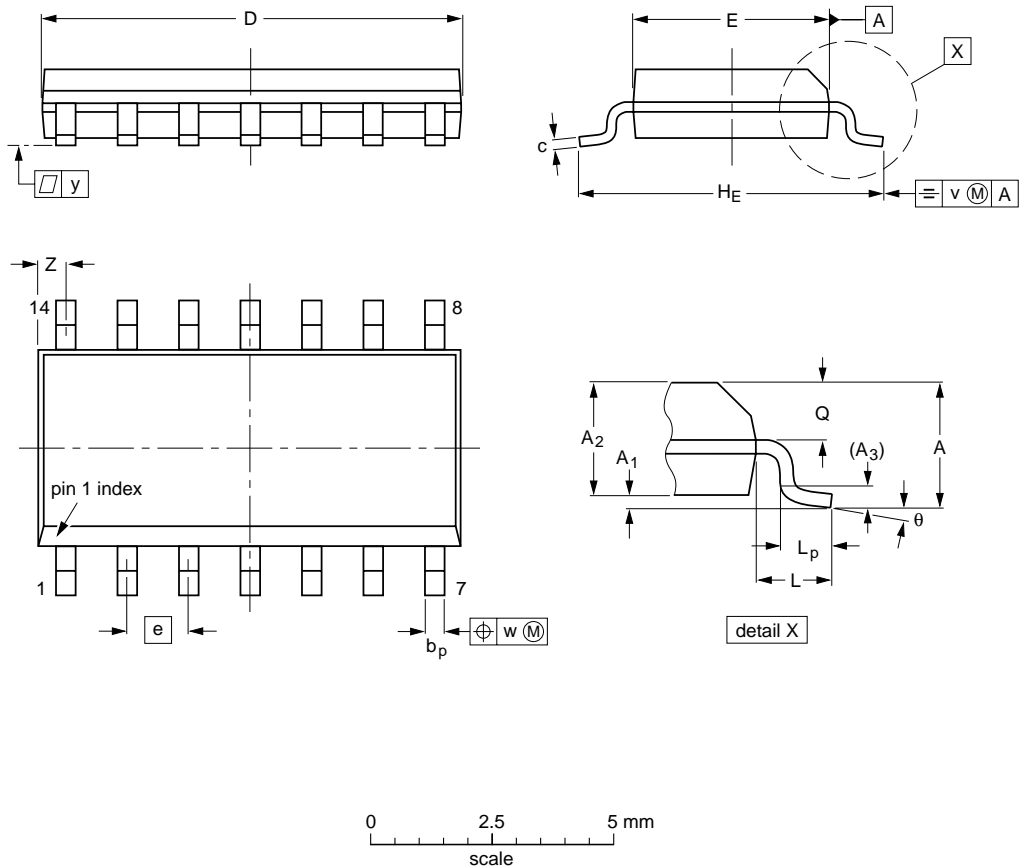
Package information

Package outlines

SO

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22

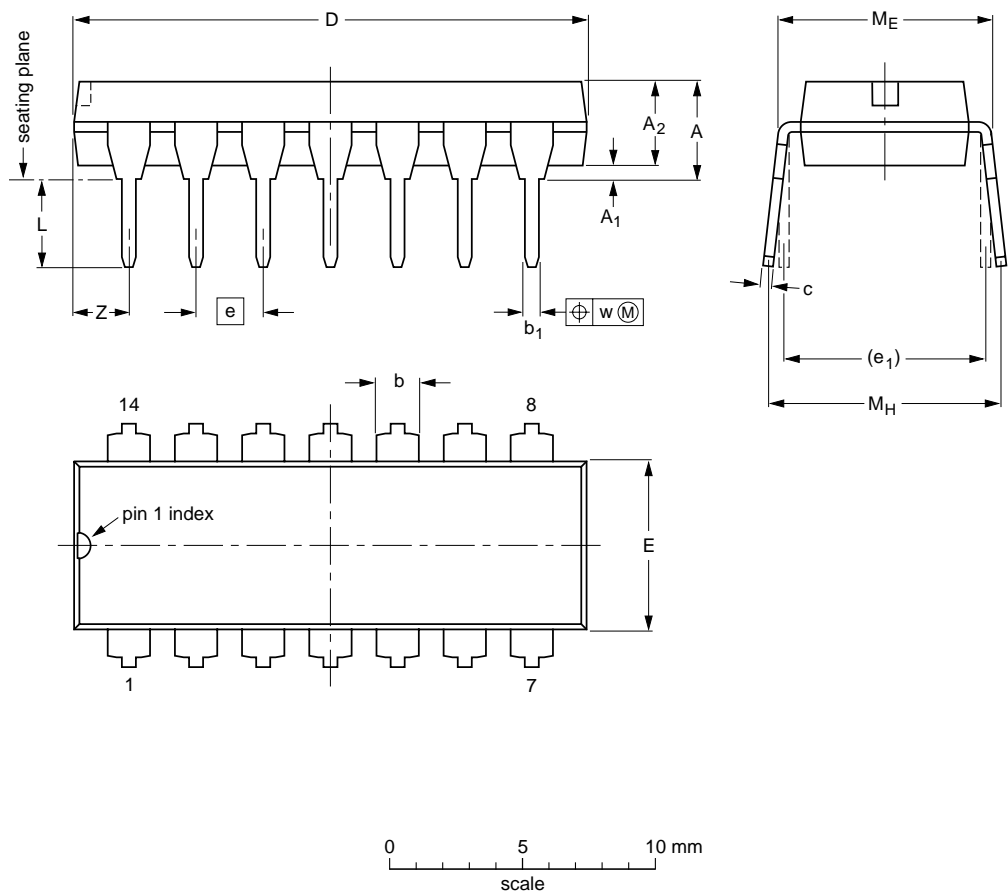
Package information

Package outlines

DIP

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11